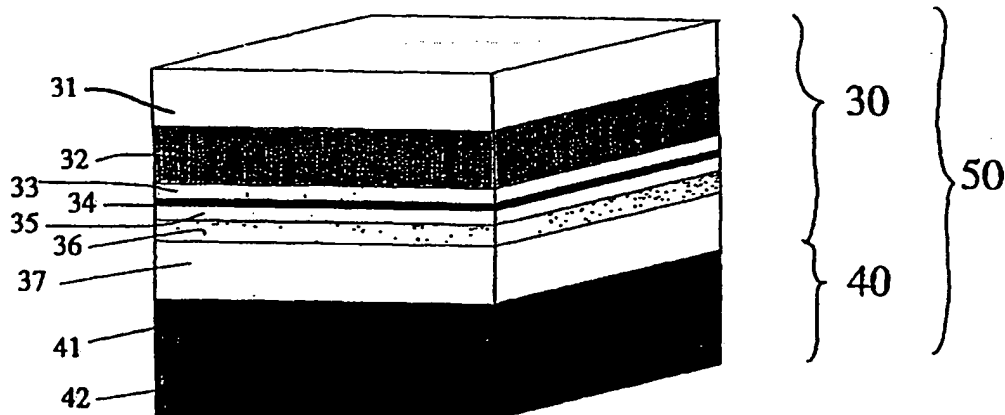




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(54) Title: **MAGNETIC STORAGE DEVICE**

## (57) Abstract

A magnetic storage device comprises an array of magnetic memory cells (50). Each cell (50) has in electrical series connection a magnetic tunnel junction (MTJ) (30) and a Zener diode (40). The MTJ (30) comprises in sequence a fixed ferromagnetic layer (FMF) (32), a non-magnetic spacer layer (33), a tunnel barrier layer (34), a further spacer layer (35), and a soft ferromagnetic layer (FMS) (36) that can change the orientation of its magnetic moment. The material type and thickness of each layer in the MTJ (40) is selected so that the cell (50) can be written by applying a voltage across the cell, which sets the orientation of the magnetic moments of the FMF (32) and FMS (36) relative to one another. The switching is effected by means of an induced exchange interaction between the FMS and FMF mediated by the tunnelling of spin-polarised electrons in the MTJ (30). The cell (50) therefore has low power consumption during write operations allowing for fast writing and dense integration of cells (50) in an array. The mechanism used to control the array to write and sense the information stored in the cells (50) is simplified.

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## **Magnetic Storage Device**

### **Description**

#### **Field of the Invention**

The present invention relates to non-volatile magnetic random access memory (MRAM) storage elements.

#### **Background of the Invention**

Important characteristics of mass information storage devices of the future should be high speed, low power consumption, low cost and small size. To achieve this aim, magnetic random access memories (MRAMs) have been proposed due to their non-volatile nature. Unlike dynamic random access memory (DRAM) cells, non-volatile memory cells such as MRAM cells do not require a complex circuitry for perpetual electronic refreshing of the information stored, and thus can in principle outperform DRAM cells in all above mentioned characteristics.

The first of such MRAMs were based on magnetic multi-layer structures, deposited on a substrate. U.S. Pat No. 5,343,422, for example, discloses a structure in which two layers of ferromagnetic material are separated by a layer of non-magnetic metallic conducting material. One of the magnetic materials, called the ferromagnetic fixed layer (FMF), has a fixed direction of magnetic moment, e.g. by having a particularly high coercive field or strong uni-axial anisotropy. The magnetisation of the other magnetic layer, called the ferromagnetic soft layer (FMS), is free to change direction between parallel and anti-parallel alignment relative to the direction of the magnetic moment of FMF.

The state of the storage element represents a logical „1“ or „0“ depending on whether the directions of the magnetic moments of the magnetic layers are aligned parallel or anti-parallel, respectively. Because the resistance levels are different for different mutual orientations of the magnetic layers, the structure acts as a spin valve. It thus allows the sensing of the state of the storage element by measuring the differential resistance  $\Delta R/R$  with a current, where  $\Delta R$  is the difference in resistance of the storage element for two different states of orientation, and  $R$  is its total resistance. Due to the high conductance of the device, strong currents are needed to obtain a high enough output voltage signal level for the sensing operation. A switching between these orientations can be achieved by passing write

currents in the vicinity of the FMS, usually by using write lines which run past the layered structure on either side. These write currents, which do not pass through the layered structure itself, induce a magnetic field at the location of the FMS which alters the orientation of the FMS, if it is stronger than the coercive field  $H_c$  of the FMS.

The main disadvantage of this set-up is the relatively high power consumption during both write and sense operations due to the high conductance of the structure. For example, conducting thin films have low sheet resistivities of about  $10\Omega/\mu\text{m}^2$  leading to cell resistances of about  $10\Omega$  for currently realisable devices. Such devices require high sense currents of the order of a  $0.1\text{mA}$  in order to get voltage signals in the region of  $1\text{mV}$ . Therefore MRAM storage devices with higher resistance have been sought for.

An alternative was proposed by *J.M. Doughton, J.Appl. Phys., 81, pp. 3758-3763 (1997)*. There, the conducting non-magnetic spacer layer between the two magnetic layers is replaced by an insulator. The device therefore forms a magnetic tunnel junction (MTJ), where spin polarised electrons tunnel through the insulator. It has a high impedance with resistivity values of  $10^4$ - $10^9\Omega/\mu\text{m}^2$ , allowing for high speed MRAMs. Further, when put into a two dimensional array such an MRAM cell can be controlled by just using two lines per cell, the minimum needed to locate the cell in such an array. Such an array, shown in Fig. 1A is proposed in U.S. 5,640,343, the disclosure of which is incorporated herein by reference.

With reference to Fig. 1A, the memory cell elements are arranged vertically between parallel electrically conductive word lines 1, 2, 3 and bit lines 4, 5, 6. This makes the device topologically simple and allows in principle for a denser array than is achievable with a similar line-width process for DRAMs. The MRAM array shown in Fig. 1A uses memory cells 9, shown in Fig. 1B, that comprise each a MTJ 8 and a p-n diode 7 in electrical series connection. The diode 7 is formed as a silicon junction with an n-type layer 10 and a p-type layer 11. It is connected by an intermediate layer 12 to the MTJ 8, which is formed as a series of stacked layers comprising a template layer 15, a first ferromagnetic layer 16, a anti-ferromagnetic layer 18 a FMF 20, a tunnelling barrier layer 22, a FMS 24 and contact layer 25.

The presence of the diode 7 in the memory cell 9 allows the use of only two lines per cell. The device can be operated such that during a sense operation only

one memory cell in the MRAM will be forward biased whereas the remaining cells will either not be biased or reverse biased. Since the reverse bias is always kept below the breakdown voltage of the diode 7, no current flows through these cells.

A cell is written by sending simultaneously a current through the word and bit line crossing at the location of the cell. Although these currents do not pass through the cell itself, the magnetic field induced by the current at the location of the FMS is strong enough to switch the orientation of the magnetic moment between its two preferred states along the easy axis of the FMS. The FMS, however, has a coercivity that is high enough such that its magnetic moment is left unchanged in this process. Similarly, in the other memory cells which lie along either the bit or word line used in the switching, the magnetic field induced by the current passing only in one line is not strong enough to switch the FMS. This set-up however still suffers from high power consumption during write operations.

As a consequence of the magnetic fields of the switching currents the density of planar integration of MJT cells in an array is also limited. Further, the supporting electric circuitry has to be designed such that both write and sense currents can be effected to flow along different paths which makes such circuitry quite complex.

### **Summary of the Invention**

In its first aspect, the present invention comprises a magnetic tunnel junction device comprising first and second stacks of layers of magnetic material, each stack comprising at least one layer, the stacks being separated by a third stack of layers of non-magnetic material, the third stack comprising at least one layer of electrically insulating material, with contacts being made to the first and second stack to apply a voltage across the device, the magnetic materials and insulating material(s) each being of a type and the said layers each having a thickness such that the orientation of the magnetic moments of said first and second stack relative to one another are changeable by applying a voltage across the device, characterised in that said orientation can be switched to a first state by applying a first voltage across the device and that said orientation can be switched to a second state applying a second voltage across the device, whereby after either switching the said orientation is maintained when a third voltage is applied to the device the said third voltage being in between the first and second voltage.

Preferably, the magnetic tunnel junction device comprises a layer of non-magnetic conductive material between at least one of the layers of magnetic material in the first or second stack and the at least one layer of insulating material in the third stack.

Preferably, a single layer of insulating material is provided to form a single tunnel barrier between the first and second stack. Alternatively, two layers of insulating material separated by a layer of non-magnetic conductive material may be provided to form a double tunnel barrier, which can be advantageous due to its special transmission characteristics.

In its second aspect the present invention comprises an array of magnetic memory cell devices, said array comprising a first plurality of conducting leads, a second plurality of conducting leads, each lead in the said second plurality crossing over each lead in the said first plurality, a plurality of magnetic memory cell devices, each magnetic memory cell device comprising in electrical series connection a diode and a magnetic tunnel junction device according to the first aspect of the present invention, each magnetic memory cell device being located at an intersection region between one of the first plurality of leads and one of the second plurality of leads, the array having means to apply a voltage to the leads in the first and second plurality such that a voltage drop across a specific memory cell device can be effected the voltage drop causing the said memory cell device to be written.

In its third aspect the present invention comprises a method of providing a magnetic tunnel junction device comprising providing a magnetic tunnel junction comprising first and second stacks of layers of magnetic material, each stack comprising at least one layer, the stacks being separated by a third stack of layers of non-magnetic material, the third stack comprising at least one layer of electrically insulating material, with contacts being made to said first and second stack to apply a voltage across the magnetic tunnel junction the type and thickness of said magnetic and insulating materials being selected such that the orientation of the magnetic moments of said first and second stack relative to one another can be changed by applying a voltage across the device, characterised in that said orientation can be switched to a first state by applying a first voltage across the device and that said orientation can be switched to a second state applying a second voltage across the device, whereby after either switching the said

orientation is maintained when a third voltage is applied to the device the said third voltage being in between the first and second voltage.

In its fourth aspect the present invention comprises a method of providing an array of magnetic memory cell devices comprising providing a first plurality of conducting leads, a second plurality of conducting leads, each lead in the said second plurality crossing over each lead in the said first plurality, a plurality of magnetic memory cell devices, each magnetic memory cell device comprising in electrical series connection a diode and a magnetic tunnel junction device according to the third aspect of the present invention, each magnetic memory cell device being located at an intersection region between one of the first plurality of leads and one of the second plurality of leads, and providing means to apply a voltage to the leads in the first and second plurality such that a voltage drop across a specific memory cell device can be effected, the voltage drop causing a magnetic field in the device through tunnelling of spin-polarised electrons which effects the device to be written by setting the orientation of the said magnetic moments relative to one another.

In this second and fourth aspect the present invention is therefore an MRAM using MTJ elements as memory cells in implementations where both write and sense currents are passing through the cell perpendicularly. The invention utilises the combined effect of the non-linear current-voltage characteristics of the tunnel process and the non-equilibrium exchange coupling between the two magnetic layers (*N.F. Schwabe et al., Physical Review B 54, pp. 12953-12968 (1996)* and *R.J. Elliott et al., Journal of Magnetism and Magnetic Materials 177-181, pp. 769-770 (1998)*).

It has been shown that when a MTJ, and preferably a MTJ comprising a non-magnetic spacer layer (NMS) between the FMS and the barrier layer and between the FMF and the barrier layer, is significantly biased out of equilibrium a strong spin polarised tunnelling current flows through the MTJ. At the same time, due to the difference in Fermi-wavevectors on either side of the MTJ, the exchange interaction changes its characteristic periodicity, and becomes a superposition of periodic functions with several wavelengths. Further, when the MTJ is biased, a strong spin-current induced exchange interaction (SCE) occurs between the magnetic layers on either side of the MTJ, which has terms that scale with the voltage and the thickness of the FMF and the FMS. This allows changing both the sign and the

strength of the exchange interaction by applying voltage across the device that is higher than a typical voltage used to sense the device.

Switching occurs when the voltage across the device is strong enough to induce a spin current across the junction which carries a magnetic field  $H_E$  across the junction that is higher than the coercive field  $H_C$  of the FMS and that has opposite sign of the alignment of the magnetic moment of the FMS. When the voltage across the MTJ is lowered again after such switching has been effected the spin-current induced magnetic field  $H_E$  sinks below the coercive field  $H_C$  of the FMS, and the FMS remains in the switched state.

In order to switch the device in the opposite direction, the MTJ has to be designed such that, when the junction is biased reverse the first time the SCE exceeds  $H_C$  of the FMS, the sign of the interaction is opposite that of the SCE when used to switch the FMS using a forward voltage. For this purpose, the MTJ has to be designed to have an asymmetric voltage-interaction response. For example the thickness of the FMS and the FMH have to be controlled such that the voltage-interaction response curve scales in relation to  $H_C$  approximately as shown in Fig. 3, where for forward voltage the first switching always occurs towards parallel alignment between the FMS and the FMF and for reverse voltage to anti-parallel alignment. Fig. 3 will be described in more detail later.

To sense the orientation of the FMS and FMF relative to one another, a weak sense voltage, that does not affect the orientation of the FMS, is applied across the device, and the resistance differential of the MTJ  $\Delta R/R$  is measured with respect to a given reference orientation similar to that in devices of the prior art.

Being able to switch the FMS by applying a voltage across the memory cell according to the present invention, rather than running strong currents past the memory cell which do not flow across the cell, substantially reduces the power consumption of the device and impedance effects in the MRAM array. Further, only having to control voltages across a memory cell according to the invention, compared with having to control both voltages across cells and currents flowing past cells, reduces the complexity of the electrical circuit driving the MRAM array.



**Specific embodiments**

Further embodiments of the present invention shall now be described with reference to the accompanying drawings in which:

Fig. 1A shows a perspective view of a MRAM array with magnetic memory cells located vertically between bit and word lines,

Fig. 1B shows an enlarged view of one of the memory cells shown in Fig. 1A,

Fig. 2 shows a perspective view of a memory cell according to the present invention,

Fig. 3 shows the exchange field – voltage response of an MTJ memory cell in relation to the coercive field  $H_c$  of the FMS according to the invention,

Fig. 4 shows schematically the diagram of the electric circuit formed by the MRAM array, and

Fig. 5 illustrates the voltage levels on the leads in the MRAM array according to the invention.

Fig. 1A and Fig. 1B have already been described.

**Construction and Operation of the Memory Cell**

The memory cell 50 in Fig. 2. is formed as a series of layers similar to the one disclosed in U.S. 5,640,343, but different in detail. In one of its preferred embodiments the cell comprises an MTJ 30 in series with a PN junction diode 40. The MTJ comprises a first contact layer 31, which can be Cu or Pt, a FMF 32 such as Co-Pt-Cr, a first NMS 33 such as Cu or Pt, a tunnelling barrier layer 34 such as MgO, a second NMS 35 such as Cu or Pt, a FMS 36 such as Ni-Fe, and a second contact layer 37 such as Cu or Pt.

The diode 40 is formed on a semiconductor substrate such as Si and contains layers of p- and n-doped Si 41 and 42, respectively. The p-doped region 41 is in contact with the second contact layer 39 and the n-doped region 42 is in contact with a word line (not shown). The initial contact layer 31 is in contact with the bit line (not shown). Preferably, the diode is formed as a Zener-diode, i.e. it can be operated through a reverse breakdown voltage in the avalanche breakdown region.

The FMF 32 and the FMS 36 are fabricated to have easy axes of magnetisation that align with one another. By using for the FMF 32 a material with particularly high anisotropy such as Co-Pt-Cr the direction of magnetisation of the easy axis of the FMF 32 is fixed against the one of the FMS 36. Alternatively, the direction of magnetisation of the FMF 32 can be set by an unidirectional anisotropy as given, for example, in U.S. 5,465,185. For the FMS 36 there are two possible directions along its easy axis, which define the two states of the memory cell. In addition the FMS may be fabricated to have a low coercivity by giving it an elliptical shape or forming tapers at the corners, giving it a hexagonal or octagonal shape, in order to suppress the effects of edge domains.

There are several differences between this embodiment and the prior art. The properties of the FMF 32 and the FMS 36 are not chosen with regard to their response to writing fields produced by external writing currents, but with regard to an optimal current-voltage characteristics facilitating both read and write operations by passing a current perpendicularly through the cell 40. The thickness and magnetic properties of the FMF 32 and the FMS 36 are chosen to achieve an asymmetric SCE which has a voltage response function such as the one shown in Fig. 3.

The construction of the tunnel barrier 34 is not only determined by the desired values for  $\Delta R/R$  to sense the state of the FMS 36, but also to accommodate switching. Due to its effect on the write performance of the device MgO is preferred as a material for the tunnel barrier 36. Alternatively, two layers of insulating material separated by a layer of non-magnetic conductive material may be provided to form a double tunnel barrier.

The presence of the NMSs 33 and 35 on one or both sides of the tunnel barrier between the FMF 32 and the tunnel barrier 34 as well as the FMS 36 and the tunnel barrier 34 is advantageous for the SCE effect as it allows the phase of the exchange interaction across the MTJ to be tuned. This is desirable to ensure that the sign of the SCE can be changed at a reasonable voltage level across the MTJ 30. The disadvantage of a very large spacer layer is, however, that the SCE decays over distance. Therefore, the right trade-off has to be achieved between appropriate phase and sufficient interaction amplitude in the optimal design of the thickness of both NMSs 33, 35.

Further advantages of the NMSs 33, 35 is that they help to reduce lattice mismatch, thus enlarging the range of possible magnetic materials, and also reduce the number of magnetic impurities in the tunnel barrier 34 which could impair the properties of the MTJ.

Further, the diode 40, formed as a Zener device, accommodates two operational regimes. One regime for the sense operation similar to the prior art, and the other one during write operations where for writing at least one of the two possible logical states a reverse voltage has to be applied to the diode 40 that is greater than its breakdown voltage.

It should be noted that although the presence of the NMSs facilitates the achievement of the desired characteristics of the MTJ their use is not strictly necessary and devices are conceivable without their use, but including the same form of operation.

Fig. 3 shows the strength of the exchange interaction, represented by the exchange field  $H_E$  versus the voltage drop  $V$  across the MTJ 30. When the voltage across the MTJ is increased from the vicinity of zero beyond the forward bias  $V_P$ , such that  $H_E > H_C$ , and lowered back again to the inception point the FMS 36 will be left in parallel alignment with the FMF 32. Similarly, when  $V$  is increased beyond  $V_{AP}$ , such that  $H_E < -H_C$ , and subsequently lowered again to close to zero, the FMS 36 and FMF 32 will be left in anti-parallel alignment. A sensing of the cell can be achieved by applying a small sensing voltage  $V_S$  across the MTJ and measuring the resistance differential  $\Delta R/R$  with respect to a given reference value.  $V_S$  is thereby substantially smaller in absolute magnitude than both  $V_P$  and  $V_{AP}$ .

It should be noted that the invention is not limited to the use of single layer FMF 32 and FMS 36, which can be replaced by stacks of magnetic layers, respectively, in order to tune the magnetic moment, anisotropy, and coercivity of these layers. Similarly the transmission characteristics of the tunnel barrier 34 can be tuned by replacing it with a double barrier structure that contains a conductive layer between two insulating layers.

#### Operation of the MRAM array

An MRAM array according to the present invention has the same topographic design as the prior art MRAM array of Fig. 1A with the difference that it contains a

memory cell according to the invention at each node in the array. A circuit diagram of the MRAM array according to the present invention is shown in Fig. 4, which is also similar to the prior art. As shown Fig. 4 the memory cells 70 to 78 lie at the intersections of the word lines 1, 2, 3 with the bit lines 4, 5, 6, which in turn are connected to the control circuits 51 and 53. Different from the operation of the prior art MRAM, however, a memory cell 70 is written by applying a strong voltage to the cell either as a forward or reverse voltage, depending on which way the cell should be switched. A voltage level diagram of the MRAM array of Fig. 4 in operation is shown in Fig. 5.

In Fig. 5 the cell 70 is first switched to a parallel alignment representing a logical „1“, then the state of cell 70 is sensed. Subsequently, the cell is switched to an anti-parallel alignment representing a logical „0“ after which the state of the cell is sensed again.

During the switching to state „1“ a voltage  $V_F$  is applied to bit line 4, using circuit 51. At the same time the voltage on bit lines 5 and 6 as well as word line 1 are set to zero, while the word lines 2 and 3 are also biased to the voltage  $V_F$  using both circuits 51 and 53. The voltage  $V_F$  across memory cell 70 induces a voltage drop  $V_P$  across the MTJ which, as shown in Fig. 3, is strong enough to switch the orientation of its FMS in the MTJ to a parallel alignment. While the cell 70 is now biased forward at  $V_F$ , cells 71, 72, 73, and 76 are unbiased and cells 74, 75, 77, 78 are reverse biased at  $-V_F$ , which is still less than the breakdown voltage of the Zener-diode and therefore does not lead to a substantial voltage drop across the MTJ.

A sensing operation is carried out by applying a voltage  $V_S$  to bit line 4, while setting the voltage on word line 1 to zero. At the same time bit lines 5,6 are kept at zero voltage whereas word lines 2,3 are biased to  $V_S$ . This way it can be seen that there will be a positive voltage drop  $V_S$  across cell 70, whereas all the other cells either have no voltage drop across them or a small reverse voltage  $-V_S$  which is smaller than the breakdown voltage of the Zener-diode.

Finally, an operation to write a logical „0“ into cell 70 is achieved by setting the voltage on bit line 4 to  $-V_R$  while setting the voltage on word line 1 to  $V_R$ . The total voltage drop across cell 70 of  $-2V_R$  is now such that it is greater than the reverse breakdown voltage of the Zener-diode and such that it induces a voltage

drop  $V_{AP}$  across the MTJ which is strong enough to switch the FMS to „0“, as indicated in Fig. 3. At the same time the voltage on bit lines 5,6 are left at zero, while the voltage on word lines 2,3 are kept at  $V_s$ . Neither of the voltage drops of  $-V_R$  and  $-V_R+V_s$  across cells 71, 72 and 73, 76, respectively are high enough to cause a reverse breakdown of the Zener-diode, thus avoiding a notable voltage drop across the relevant MTJs.

In the embodiment of the MRAM array described above, voltages are applied using the control circuits 51,53, such that during either a read or write operation only one cell will be addressed at any one time and the power consumption of the device is kept to a minimum. The method of applying voltages described here is merely an example to which the invention is not limited, and other combinations of applying voltages for operating a memory cell and the MRAM array are conceivable.

**Claims**

1. A magnetic tunnel junction device comprising first and second stacks of layers of magnetic material, each stack comprising at least one layer, the stacks being separated by a third stack of layers of non-magnetic material, the third stack comprising at least one layer of electrically insulating material, with contacts being made to the first and second stack to apply a voltage across the device, the magnetic materials and insulating material(s) each being of a type and the said layers each having a thickness such that the orientation of the magnetic moments of said first and second stack relative to one another are changeable by applying a voltage across the device, characterised in that said orientation can be switched to a first state by applying a first voltage across the device and that said orientation can be switched to a second state applying a second voltage across the device, whereby after either switching the said orientation is maintained when a third voltage is applied to the device the said third voltage being in between the first and second voltage.
2. A device as claimed in Claim 1 in which at least one of the said first and second stacks is separated from the third stack by a further layer of non-magnetic conducting material.
3. A device as claimed in Claim 1 or Claim 2 in which the third stack comprises two layers of insulating material separated from one another by a layer of non-magnetic conductive material.
4. A device as claimed in any preceding Claim in which at least one of the layers of magnetic material in the said first or second stack has a substantially elliptical shape.
5. A device as claimed in Claims 1, 2 or 3 in which at least one of the layers of magnetic material in the said first or second stack has a substantially hexagonal or octagonal shape.
6. A device as claimed in any preceding Claim in which the easy axes of the magnetisation of the said first and second stack are aligned with one another such that the orientation of the magnetic moments of said first and second stack relative to one another are changeable between substantially parallel and substantially anti-parallel states.

7. A device as claimed in Claim 6 with the magnetic materials and insulating material(s) each being of a type and the said layers each having a thickness thus causing an asymmetric current response such that the changing from substantially parallel to substantially anti-parallel state is allowed to be effected by applying a forward or backward voltage to the device, wherein the change effected by applying a forward voltage is opposite to the change effected by applying a backward voltage.
8. A device as claimed in any preceding Claim comprising sensing means connected to the said contacts which allows the orientation of the magnetic moments of said first and second stack relative to one another to be sensed by applying a fourth voltage across the device and measuring the resistance of the device.
9. A device as claimed in Claim 8 in which the fourth voltage applied to the device in order to sense the state of the device is smaller in absolute terms than a voltage applied to the device in order to change the state of the device.
10. A device as claimed in any preceding claim in which the said third stack comprises at least one layer of manganese oxide (MgO).
11. A device as claimed in Claim 10 in which the easy axes of the magnetisation of the said first and second stack are aligned with one another such that the device can be switched between two states in which the orientation of the magnetic moments of said first and second stack can be changed from a substantially parallel alignment to substantially anti-parallel alignment by applying one of the said first and second voltages to the device and said magnetic moments can be switched from a substantially anti-parallel alignment to a substantially parallel alignment by applying the other of the said first and second voltages to the device.
12. A magnetic memory cell device comprising a magnetic tunnel junction device as claimed in any preceding Claim which comprises a diode in electrical series connection with the magnetic tunnel junction device.
13. A magnetic memory cell device as in Claim 12 wherein the diode is a Zener diode.
14. A device as claimed in Claim 12 or Claim 13 having means allowing to effect one of the said voltages required to switch the relative orientation of the magnetic moments of the said first and second stacks in the magnetic tunnel junction device

by allowing to apply a further voltage across the magnetic memory cell device said further voltage effecting a voltage across the diode which is a reverse voltage on the diode, said reverse voltage being greater than the breakdown voltage of the diode.

15. An array of magnetic memory cell devices comprising a first plurality of conducting leads, a second plurality of conducting leads, each lead in the said second plurality crossing over each lead in the said first plurality, a plurality of magnetic memory cell devices as claimed in Claim 12 to Claim 14, each magnetic memory cell device being located at an intersection region between one of the first plurality of leads and one of the second plurality of leads, the array having means to apply a voltage to the leads in the first and second plurality such that a voltage drop across a specific memory cell device can be effected, the voltage drop causing the said memory cell device to be written by setting the orientation of said magnetic moments relative to one another.

16. A method of providing a magnetic tunnel junction device comprising providing a magnetic tunnel junction comprising first and second stacks of layers of magnetic material, each stack comprising at least one layer, the stacks being separated by a third stack of layers of non-magnetic material, the third stack comprising at least one layer of electrically insulating material, with contacts being made to said first and second stack to apply a voltage across the magnetic tunnel junction the type and thickness of said magnetic and insulating materials being selected such that the orientation of the magnetic moments of said first and second stack relative to one another can be changed by applying a voltage across the device, characterised in that said orientation can be switched to a first state by applying a first voltage across the device and that said orientation can be switched to a second state applying a second voltage across the device, whereby after either switching the said orientation is maintained when a third voltage is applied to the device the said third voltage being in between the first and second voltage.

17. A method as claimed in Claim 16 comprising providing two layers of insulating material in the said third stack, which two layers of insulating material are separated from one another by a layer of non-magnetic conductive material.



18. A method as claimed in Claim 16 or Claim 17 in which at least one of the layers of magnetic material in the said first or second stack is provided having a substantially elliptical shape.
19. A method as claimed in Claims 16 to 17 in which at least one of the layers of magnetic material in the said first or second stack is provided having a substantially hexagonal or octagonal shape.
20. A method as claimed in Claims 16 to 19 comprising providing a layer of non-magnetic conductive material between the said third stack and at least one of the said first and second stacks.
21. A method as claimed in Claim 16 to Claim 20 in which the orientation of the magnetic moments of said first and second stack relative to one another can be changed between substantially parallel and substantially anti-parallel states.
22. A method as claimed in Claim 21 in which changing from substantially parallel to substantially anti-parallel state is effected by applying a forward or backward voltage to the device, wherein the change effected by applying a forward voltage is opposite the change effected by applying a backward voltage.
23. A method as claimed in Claims 16 to 22 in which the orientation of the magnetic moments of said first and second stack relative to one another can be sensed by applying a fourth voltage across the magnetic tunnel junction device and measuring the resistance of the device.
24. A method as claimed in Claim 23 in which the fourth voltage applied to the device in order to sense the orientation of the magnetic moments of the said first and second stack relative to one another is smaller in absolute terms than the voltage applied to the device in order to change the relative alignment of said magnetic moments.
25. A method as claimed in any preceding Claim in which the said third stack is provided with at least one layer of manganese oxide (MgO).
26. A method as claimed in Claim 25 in which the device can be switched between two states in which the orientation of the magnetic moments of said first and second stack can be changed from a substantially parallel alignment to substantially anti-parallel alignment by applying on of the said first and second voltages to the device and said magnetic moments can be switched from a

substantially anti-parallel alignment to a substantially parallel alignment by applying the other of the said first and second voltages to the device.

27. A method of providing magnetic memory cell device comprising providing a magnetic tunnel junction device as claimed in any of Claims 16 to 25 which comprises providing a diode in electrical series connection with the magnetic tunnel junction device.

28. A method as claimed in Claim 27 wherein the diode is a Zener diode.

29. A method as claimed in Claim 27 or Claim 28 in which one of the said voltages required to switch the relative orientation of the magnetic moments of said first and second stack in the magnetic tunnel junction device is effected by applying a further voltage across the magnetic memory cell device said further voltage effecting a voltage across the diode which is a reverse voltage on the diode, said reverse voltage being greater than the breakdown voltage of the diode.

30. A method of providing an array of magnetic memory cell devices comprising providing a first plurality of conducting leads, a second plurality of conducting leads, each lead in the said second plurality crossing over each lead in the said first plurality, a plurality of magnetic memory cell devices provided as claimed in Claim 27 to Claim 29, each magnetic memory cell device being located at an intersection region between one of the first plurality of leads and one of the second plurality of leads, and providing means to apply a voltage to the leads in the first and second plurality such that a voltage drop across a specific memory cell device can be effected, the voltage drop causing a magnetic field in the device through tunnelling of spin-polarised electrons which effects the device to be written by setting the orientation of the said magnetic moments relative to one another.

31. A magnetic tunnel junction device substantially as herein before described with reference to Figure 2 to Figure 5 of the accompanying drawings.

32. A magnetic memory cell device substantially as herein before described with reference to Figure 2 to Figure 5 of the accompanying drawings.

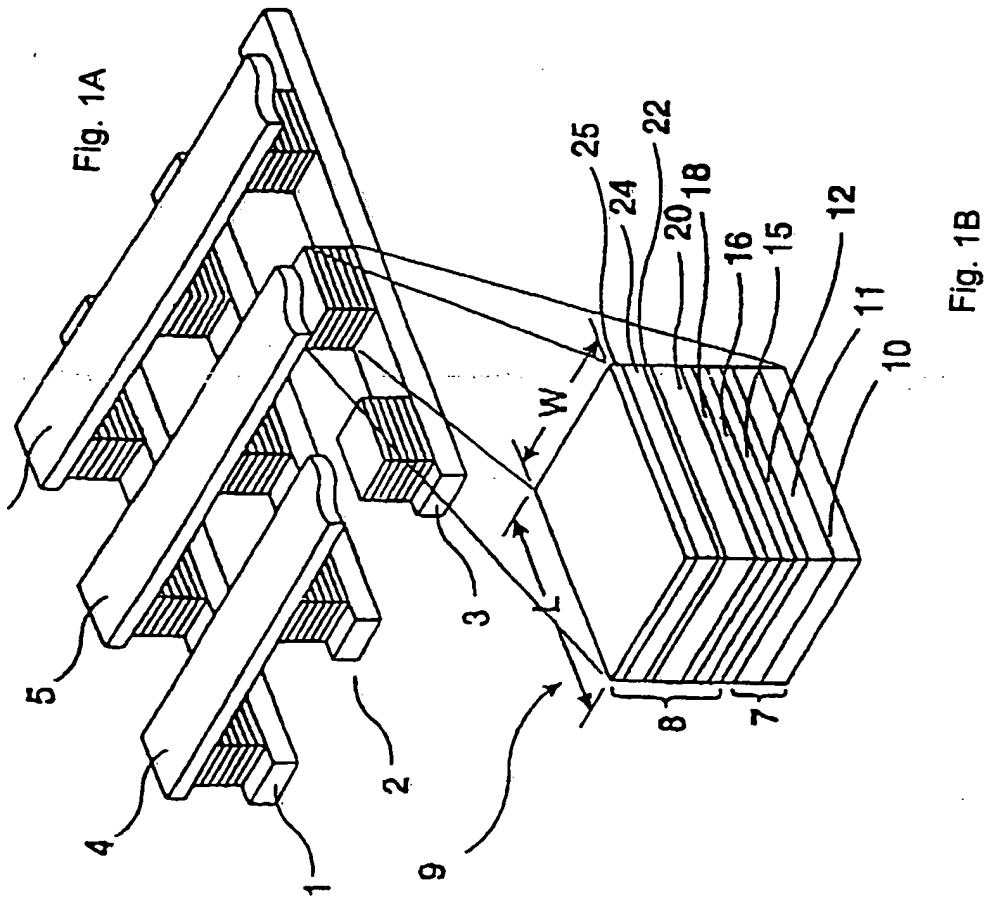
33. A magnetic memory cell array substantially as herein before described with reference to Figure 2 to Figure 5 of the accompanying drawings.

34. A method of providing a magnetic tunnel junction device substantially as herein before described with reference to Figure 2 to Figure 5 of the accompanying drawings.

35. A method of providing a magnetic memory cell device substantially as herein before described with reference to Figure 2 to Figure 5 of the accompanying drawings.

36. A method of providing a magnetic memory cell array substantially as herein before described with reference to Figure 2 to Figure 5 of the accompanying drawings.

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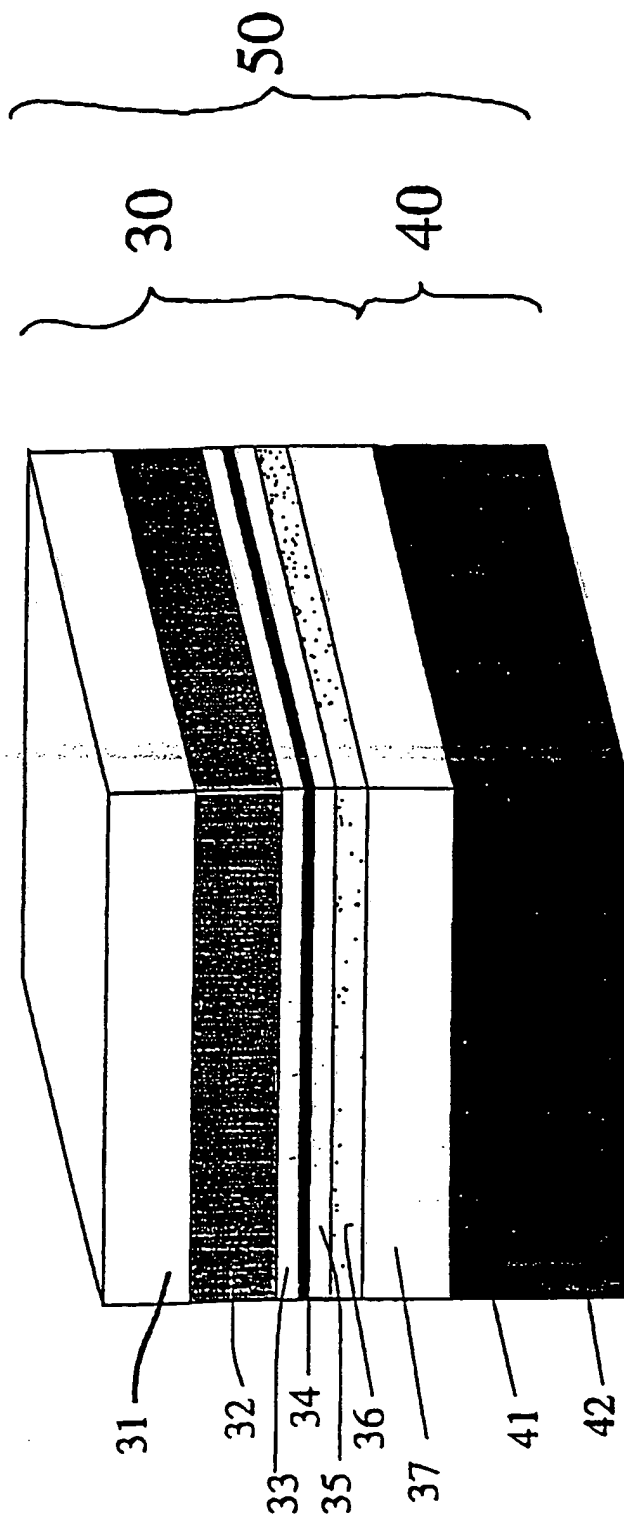


Fig. 2

Fig. 3

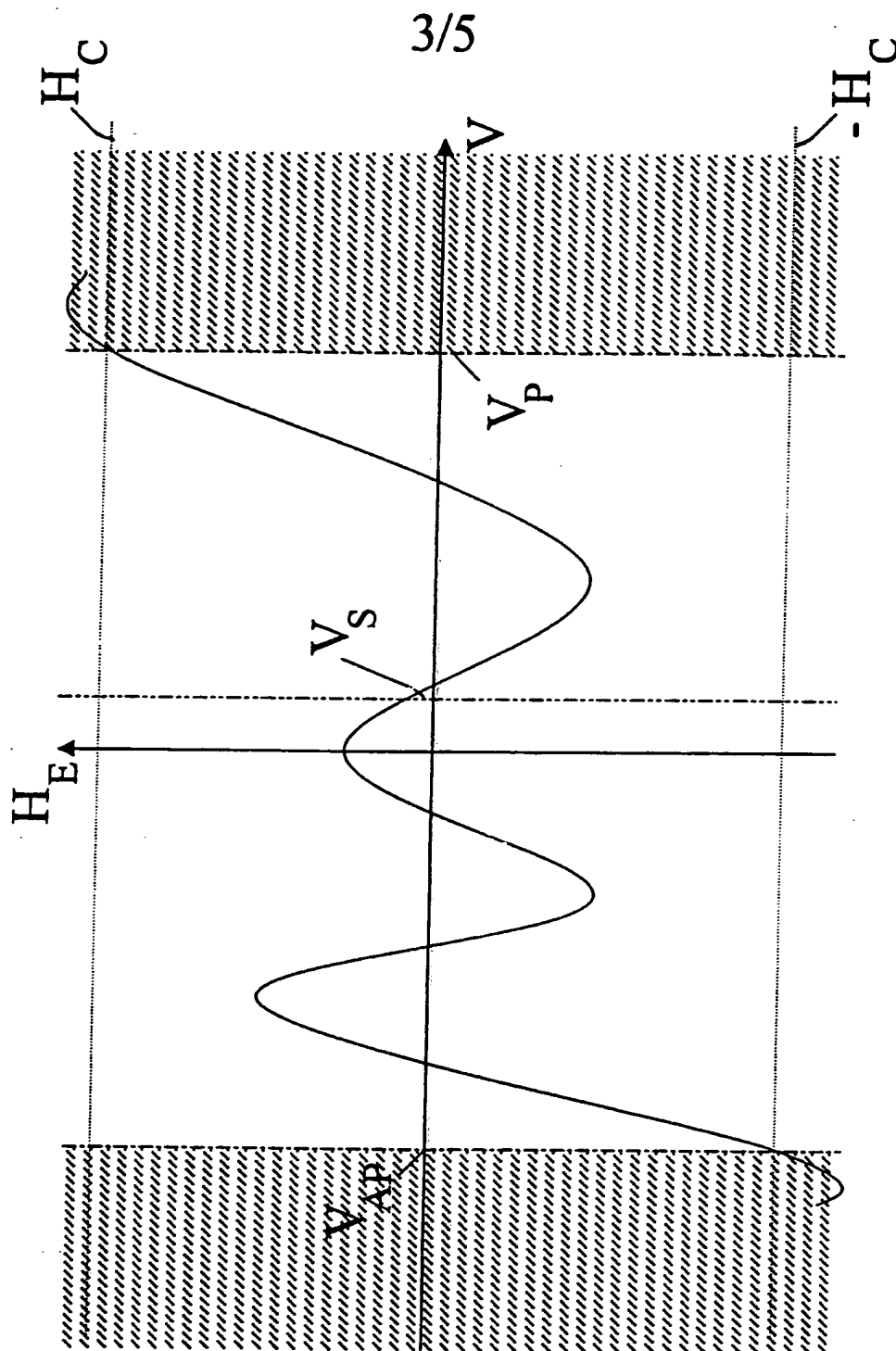
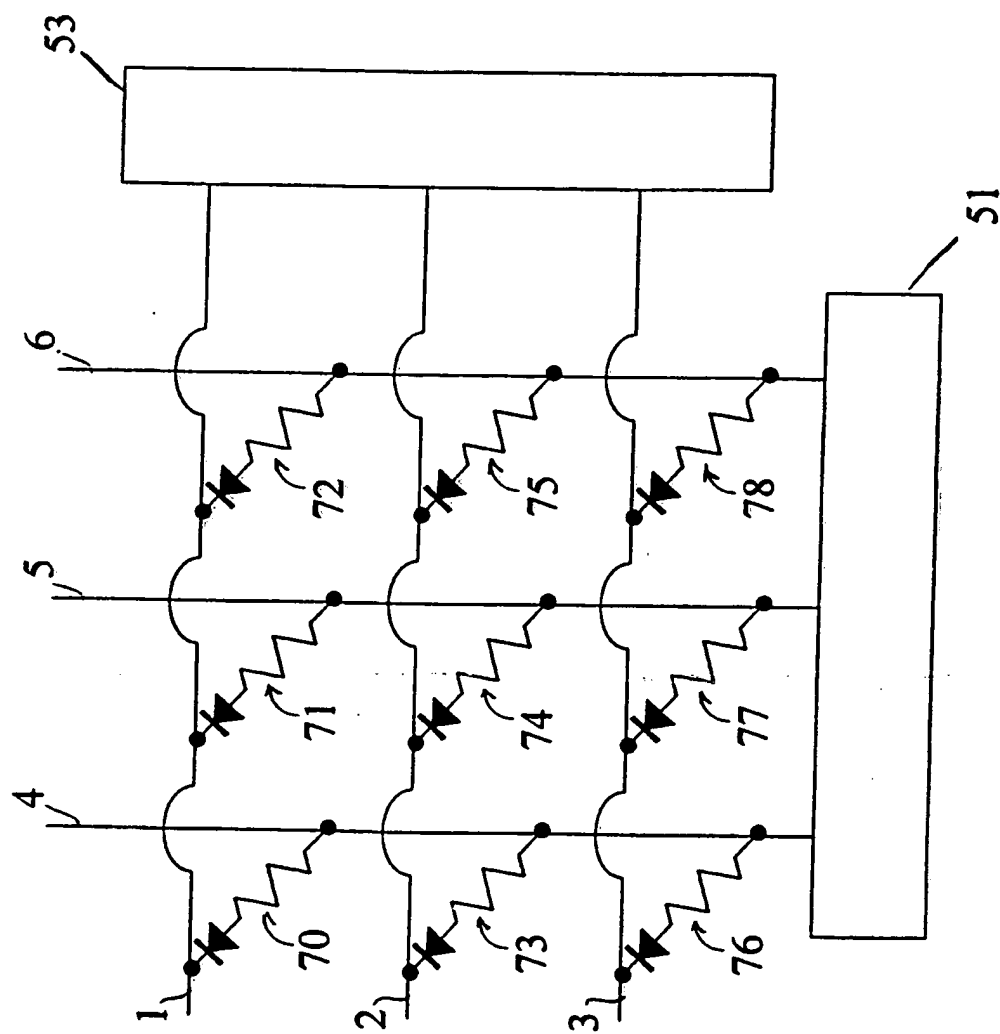
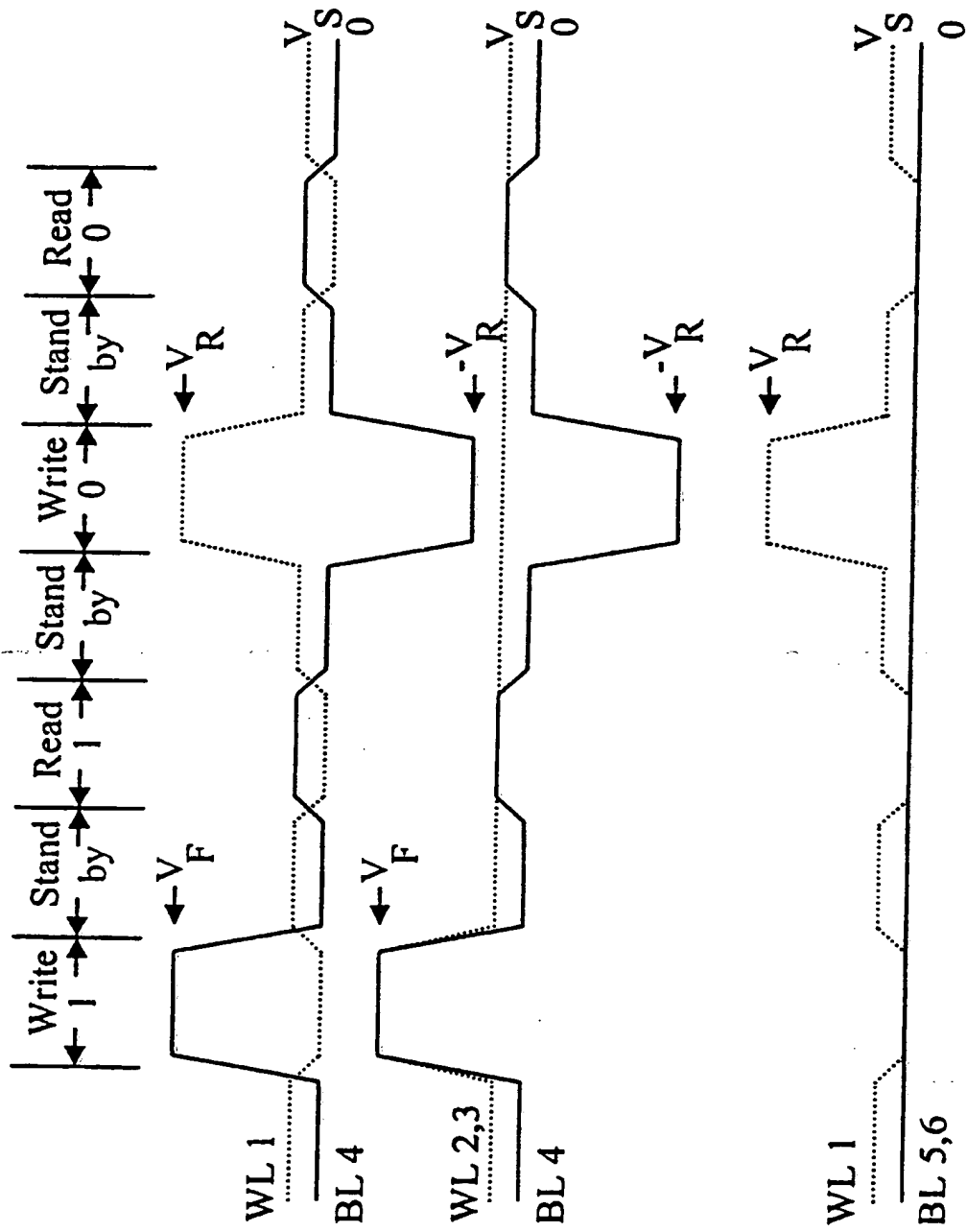


Fig. 4



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Fig. 5





# INTERNATIONAL SEARCH REPORT

Int. onal Application No

PCT/EP 99/08368

## A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 G11C11/16

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	US 5 835 314 A (MOODERA JAGADEESH S ET AL) 10 November 1998 (1998-11-10)	1,2,4,6, 7,9-11, 16,18, 21-26 5,8,19
P,A	column 6, line 37 -column 10, line 28 column 11, line 64 -column 12, line 13 & WO 97 39488 A	
A	US 5 764 567 A (PARKIN STUART STEPHEN PAPWORTH) 9 June 1998 (1998-06-09) column 6, line 57 -column 10, line 49	1

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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Date of the actual completion of the international search

22 March 2000

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29/03/2000

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# INTERNATIONAL SEARCH REPORT

Information on patent family members

Int. onal Application No

PCT/EP 99/08368

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		EP 0894342 A	03-02-1999
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